PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

KAWABATA et al. Art Unit: 2818

Application No.: 09/994,610 Examiner: L. Pham

Filed: November 28, 2001 Attorney Dkt. No.: 100353-00086

For: SEMICONDUCTOR INTEGRATED CIRCUIT

REQUEST FOR RECONSIDERATION UNDER 37 CFR § 1.111

Commissioner for Patents
Washington, D.C. 20231 April 21, 2003

Sir:

The Office Action dated December 19, 2002, has been received and carefully noted. The period for response having been extended from March 19, 2003 to April 21, 2003 (April 19, 2003 being a Saturday), by the attached Petition for Extension of Time, the following remarks are submitted as a full and complete response thereto.

Applicants acknowledge the withdrawal of claims 7-20, as noted in the Office Action. No amendments have been made, and therefore no new matter is added. Accordingly, claims 1-6, as originally filed, are pending in the present application, and are respectfully submitted for reconsideration.

Claims 1-3 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Furutani et al. (U.S. Patent No. 5,305,261, hereinafter "Furutani") in view of Padgett (U.S. Patent No. 4,079,332). In making this rejection, the Office Action took the position that Furutani disclosed each and every element recited in the claimed invention with the

exception of showing operating modes having a dynamic operation mode in which the signal lines are precharged, and a static operation mode in which the signal lines are not precharged. The Examiner cites Padgett for curing the deficiencies which exist in Furutani. Applicants respectfully traverse this rejection, and submit that each of claims 1-3 recites subject matter that is neither disclosed nor suggested in the cited prior art.

It is noted that claims 4-6 were not specifically rejected in the Office Action. However, Applicants shall address and respond to the comments made with respect to claims 4-6 within the Office Action.

Claim 1 recites a semiconductor device having signal lines over which signals are transferred, and a drive circuit driving the signal lines in operating modes. The operating modes include a dynamic operation mode in which the signal lines are precharged, and a static operation mode in which the signal lines are not precharged.

Accordingly, one of the essential features of the present invention is a semiconductor device having at least a drive circuit for driving the signal lines in operating modes, where the "operating modes include a dynamic operation mode in which the signal lines are precharged and a static operation mode in which the signal lines are not precharged." As such, the present invention results in the advantage of having a semiconductor integrated circuit device in which a circuit for driving signals has a reduced configuration and where the chip area occupied by the circuit can be reduced.

It is respectfully submitted that the prior art fails to disclose or suggest the elements of the Applicants' invention as set forth in claims 1-3,and therefore fails to provide the advantages which are provided by the present invention.

Furutani discloses a semiconductor memory device having an internal data transmitting line for transmitting both of internal write data and internal read data, a memory cell array including a plurality of memory cells arranged in a matrix, column selecting circuitry which is responsive to an applied address signal to generate a column selecting signal for selecting a corresponding column in the memory cell array, and column connecting circuitry which is responsive to the column selecting signal for connecting the corresponding column line to the internal data transmitting line. In addition, the semiconductor memory device of Furutani includes an amplifying circuit which is provided for each column line to detect and amplify a potential on the corresponding column line.

Padgett discloses a MOSFET high gain differential amplifier circuit having a pair of cascade connected inverter stages, each stage connected to a source of relatively positive reference potential. Each inverter stage has an input and output terminal and is comprised of a series of connected depletion modes FET device and an enhancement mode FET device. An additional enhancement mode FET device is connected between a source of relatively negative reference potential, such as ground, and a common electrical junction formed by the inverter stages. The positive feedback cap is connected between the output terminal of a first inverter stage and the control electrode

of the additional FET, whereby the current in each inverter stage is controlled. A high gain signal is achieved at the output terminal of the second inverter stage.

Applicants respectfully submit that each and every element recited within claim 1 is neither disclosed nor suggested by Furutani and/or Padgett, taken alone or in combination. In particular, Applicants submit that the semiconductor device as recited in the present application is clearly distinct from that which is illustrated by the combination of the cited prior art. Specifically, it is submitted that the cited prior art fails to disclose or suggest operating modes that include a dynamic operation mode in which the signal lines are precharged, and a static operation mode in which the signal lines are not precharged.

As noted on page 3 of the Office Action, the Examiner admits that Furutani fails to disclose or suggest the limitation of "the operating modes including a dynamic operation mode in which the signal lines are precharged, and a static operation mode in which the signal lines are not precharged", as recited in claim 1 of the present application. The Office Action cited Padgett for curing the above deficiencies which exist in Furutani.

Padgett merely discloses a dynamic operating mode in the Background of the Invention section of the reference, and a static operating mode within the main body section of the reference. The dynamic operating mode as disclosed in Padgett functions by itself without the existence of the static operating mode. Similarly, the static operating mode as shown in Padgett operates by itself without the existence of the dynamic operating mode. Therefore, Padgett merely discloses using only one of the

two operating modes. Accordingly, Padgett fails to disclose or suggest the primary feature of using both operating modes including the dynamic operating mode and the static operating mode as provided by the present invention.

Furthermore, the subject matter disclosed by Padgett uses the static operating mode to overcome the drawbacks of the dynamic operating mode, thereby avoiding an increase in the size and cost of the amplifier circuit. Therefore, Applicants respectfully submit that Padgett teaches away from the dynamic operating mode, and there is no motivation or suggestion to use both the dynamic operating mode and the static operating mode in one single semiconductor device as provided in the present invention. Accordingly, Applicants respectfully submit that neither Furutani and/or Padgett, taken alone or in combination, disclose or suggest each and every element recited within claim 1 of the present invention.

As for claims 2-6, Applicants submit that each of these claims recites subject matter which is neither disclosed nor suggested in the cited prior art. In particular, each of these claims depends on claim 1. Therefore, each of claims 2-6 incorporates each and every limitation recited within claim 1 therein. Therefore, Applicants submit that each of claims 2-6 also recites subject matter that is neither disclosed nor suggested by Furutani and/or Padgett, taken alone or in combination, for at least the reasons set forth above with respect to claim 1.

In view of the above, Applicants respectfully submit that claims 1-6 each recites subject matter which is neither disclosed nor suggested in the cited prior art. Applicants also submit that this subject matter is more than sufficient to render the claims non-

obvious to a person of ordinary skill in the art, and therefore respectfully request that claims 1-6 be found allowable and that this application be passed to issue.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact by telephone the Applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper has not been timely filed, Applicant respectfully petitions for an appropriate extension of time. The Commissioner is authorized to charge payment for any additional fees which may be required with respect to this paper to Counsel's Deposit Account 01-2300, referring to Attorney Docket number 100353-00086.

Respectfully submitted,

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Enclosures: Petition for Extension of Time (one month)